Patent claims

1. A method for fabricating a plurality of semiconductor bodies, comprising:

(a) forming a mask layer (3) over a substrate (1) or over an initial layer (2), which mask layer has a plurality of windows (4) leading to the substrate (1) or to the initial layer (2) and onto which mask layer a semiconductor material (5), which is to be grown onto the substrate (1) in a subsequent method step, substantially cannot be grown or can be grown to a significantly reduced extent by comparison with the substrate (1) or the initial layer (2),

(b) etching back the substrate (1) or the initial layer (2) in the windows (4), in such a manner that pits (41) are formed in the substrate (1) or in the initial layer (2) starting from these windows,

(c) growing the semiconductor material (5) onto the substrate (1) or onto the initial layer (2), in such a manner that lateral growth is promoted and the semiconductor material initially grows primarily from the flanks (43) of the pits (41) toward the center (42) of the pits (41) where they form a coalescence region (61), so that defects in the substrate (1) or in the initial layer (2) which impinge on the flanks (43) of the pits (41) bend off toward the center of the pits (41) in the semiconductor material, and then, starting from the windows (4), grows over the mask layer (3) and in each case grows together over the mask layer (3) between adjacent windows

(4), where it forms a further coalescence region (62), and

(d) growing a component layer sequence (8) onto the semiconductor material (5).

2. The method as claimed in claim 1, in which the growth of the semiconductor material (5) is effected by means of metalorganic vapor phase epitaxy in an epitaxy reactor (9) and mask material is applied to the substrate (1) or to the initial layer (2) in the epitaxy reactor (9) in such a manner that a discontinuous mask layer (3) is formed, in which the windows (4) leading to the substrate (1) or to the initial layer (2) are already formed during the deposition of the mask layer (3).

3. The method as claimed in claim 2, in which if present the initial layer (2) is likewise applied to the substrate (1) in situ while it is in the epitaxy reactor (9).

4. The method as claimed in claim 1, in which a cross section of the pits (41) perpendicular to the plane of the substrate is preferably formed in a V shape and/or a U shape.

5. The method as claimed in claim 1, in which the semiconductor material (5) includes a plurality of layers of different compositions.

6. The method as claimed in claim 1, in which the semiconductor material (5) is grown on using an ELOG technique.

7. The method as claimed in claim 1, in which the semiconductor material (5) which has grown on has a substantially planar surface (7).

8. The method as claimed in claim 1, in which the mask layer (3) has a lattice-like or mesh-like structure.

9. The method as claimed in claim 1, in which the mask layer (3) contains silicon nitride.

10. The method as claimed in claim 1, in which the semiconductor material (5) and/or the component layer sequence contains a compound of elements from the main groups III and V.

11. The method as claimed in claim 1, in which the semiconductor material (5) and/or the component layer sequence (8) contains a nitride compound semiconductor material.

12. The method as claimed in claim 1, in which the semiconductor material (5) contains a composition selected from the system $In_xAl_yGa_{1-x-y}N$, where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x + y \leq 1$.

13. The method as claimed in claim 1, in which the substrate (1) contains silicon, silicon carbide and/or sapphire.

14. An electronic semiconductor body, which is fabricated using the method as claimed in claim 1.

15. The electronic semiconductor body as claimed in claim 14, which is a radiation-emitting semiconductor chip, in particular a light-emitting diode chip or a laser diode chip.

16. The method as claimed in claim 1, wherein the plurality of semiconductor bodies are based on nitride compound semiconductor material.

17. A method for fabricating a plurality of semiconductor bodies, comprising:

(a) forming a mask layer over an underlying layer, wherein said mask layer has a plurality of windows onto the underlying layer, and wherein said underlying layer comprises at least one of a substrate and an initial layer;

(b) etching, through the windows in the mask layer, pits in the underlying layer; and

(c) depositing a semiconductor material by:

(i) growing said semiconductor material laterally from flanks of said pits in the underlying layer, wherein first coalescence regions are formed substantially in the center of each of said pits, wherein defects in the underlying layer which contact the sides of said pits propagate in said semiconductor material in a lateral direction toward said first coalescence regions; and

(ii) growing said semiconductor material outward from said windows, as said windows become full of deposited semiconductor material, over said mask layer, wherein second coalescence regions are formed above said mask layer.

18. The method as claimed in claim 17, wherein the plurality of semiconductor bodies are based on nitride compound semiconductor material.

19. The method as claimed in claim 17, further comprising forming a layer of said semiconductor material above both said mask layer and said pitted underlying layer

20. The method as claimed in claim 19, further comprising forming a substantially planar surface on said layer.

21. The method as claimed in claim 17, further comprising growing a sequence of component layers on said substantially planar surface.